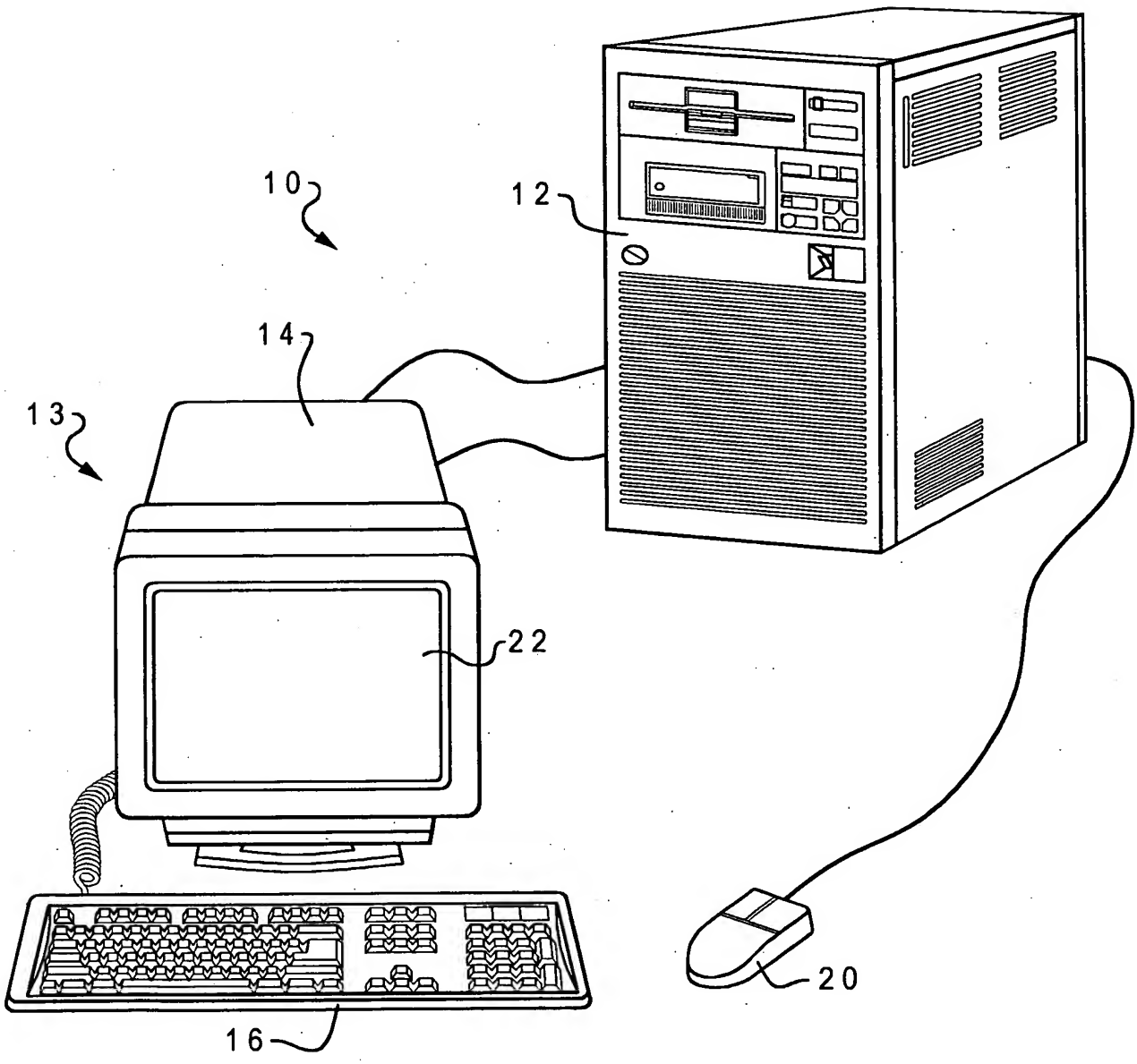

Fig. 1
Prior Art

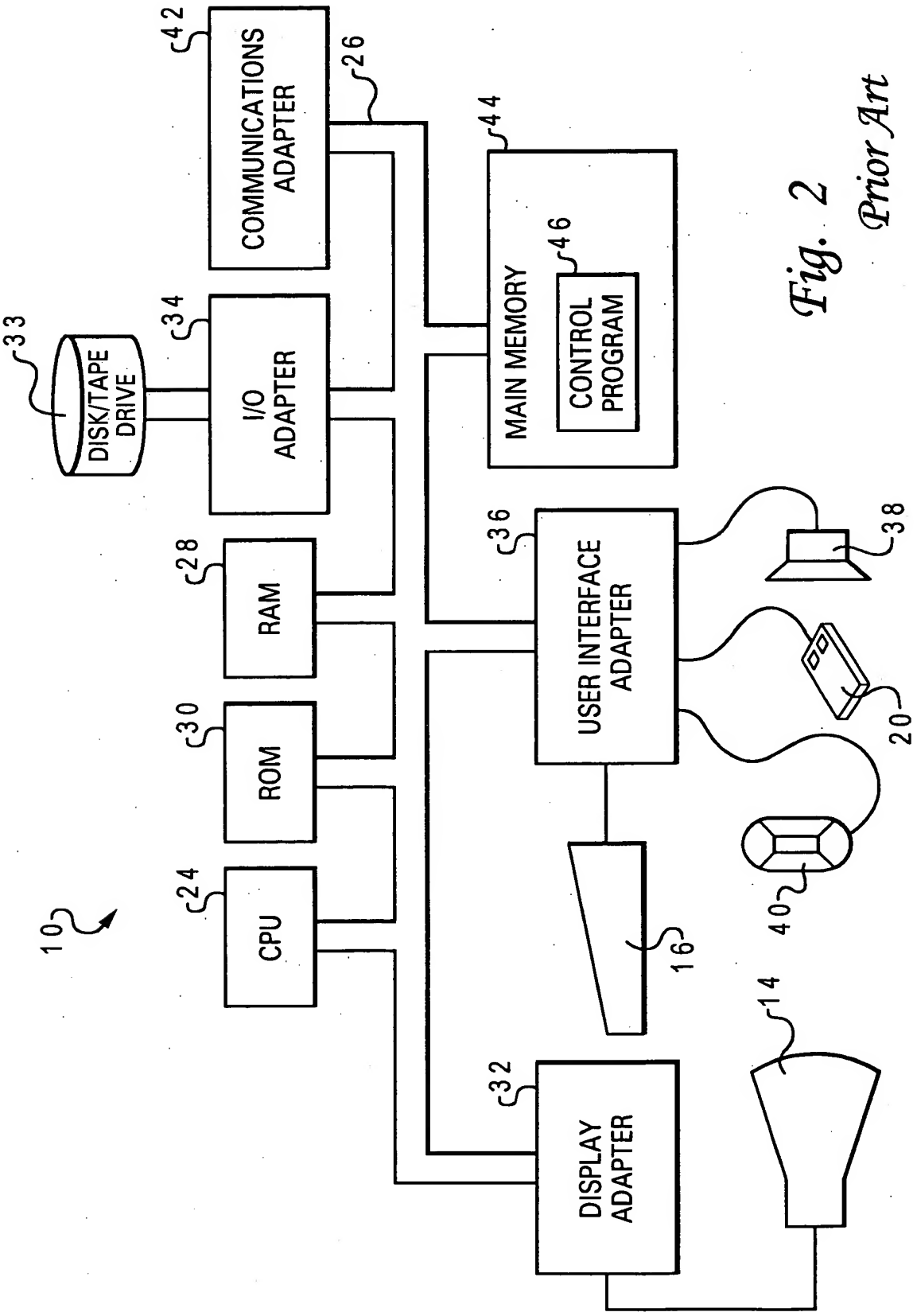

Fig. 2
Prior Art

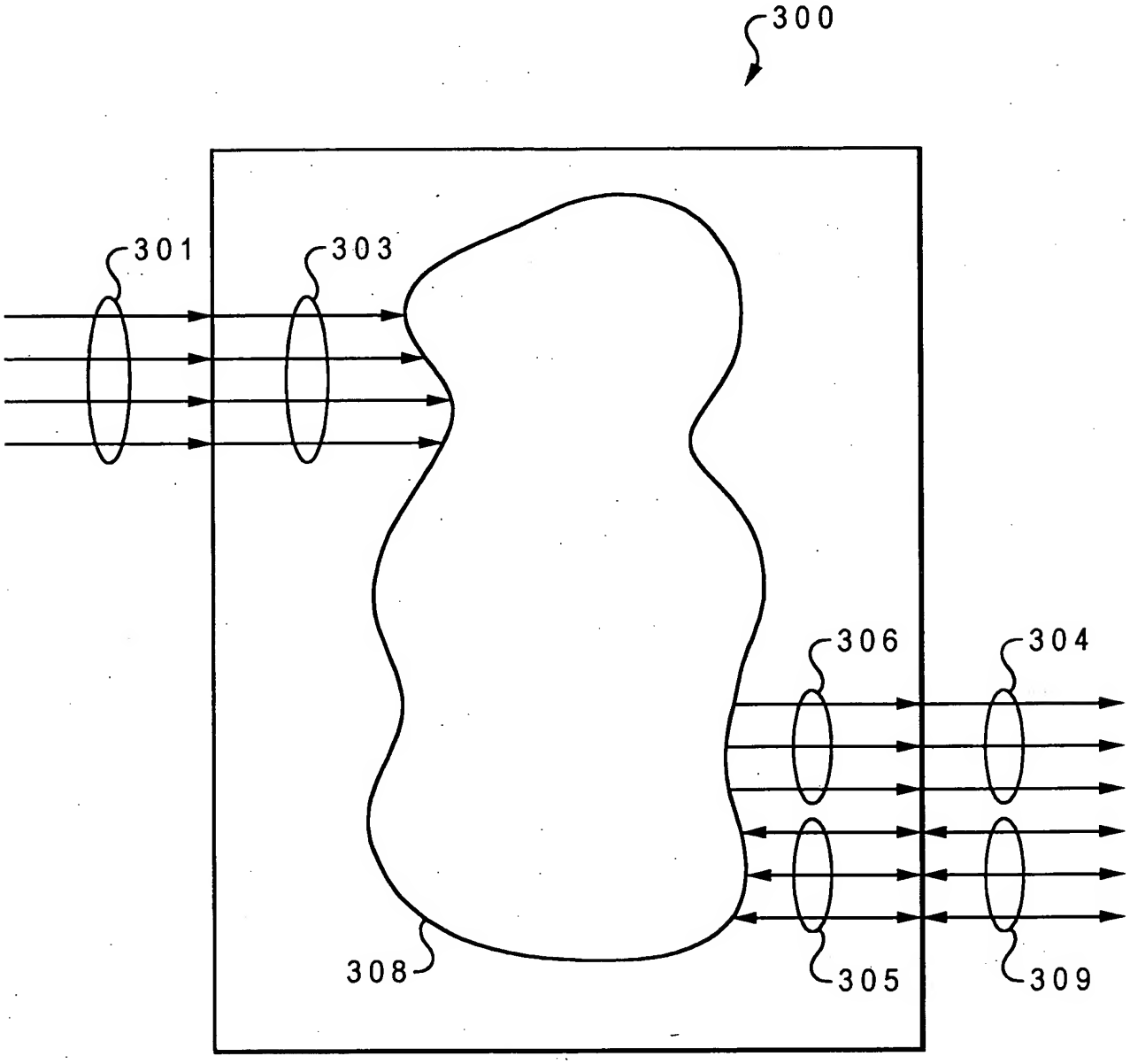

Fig. 3A

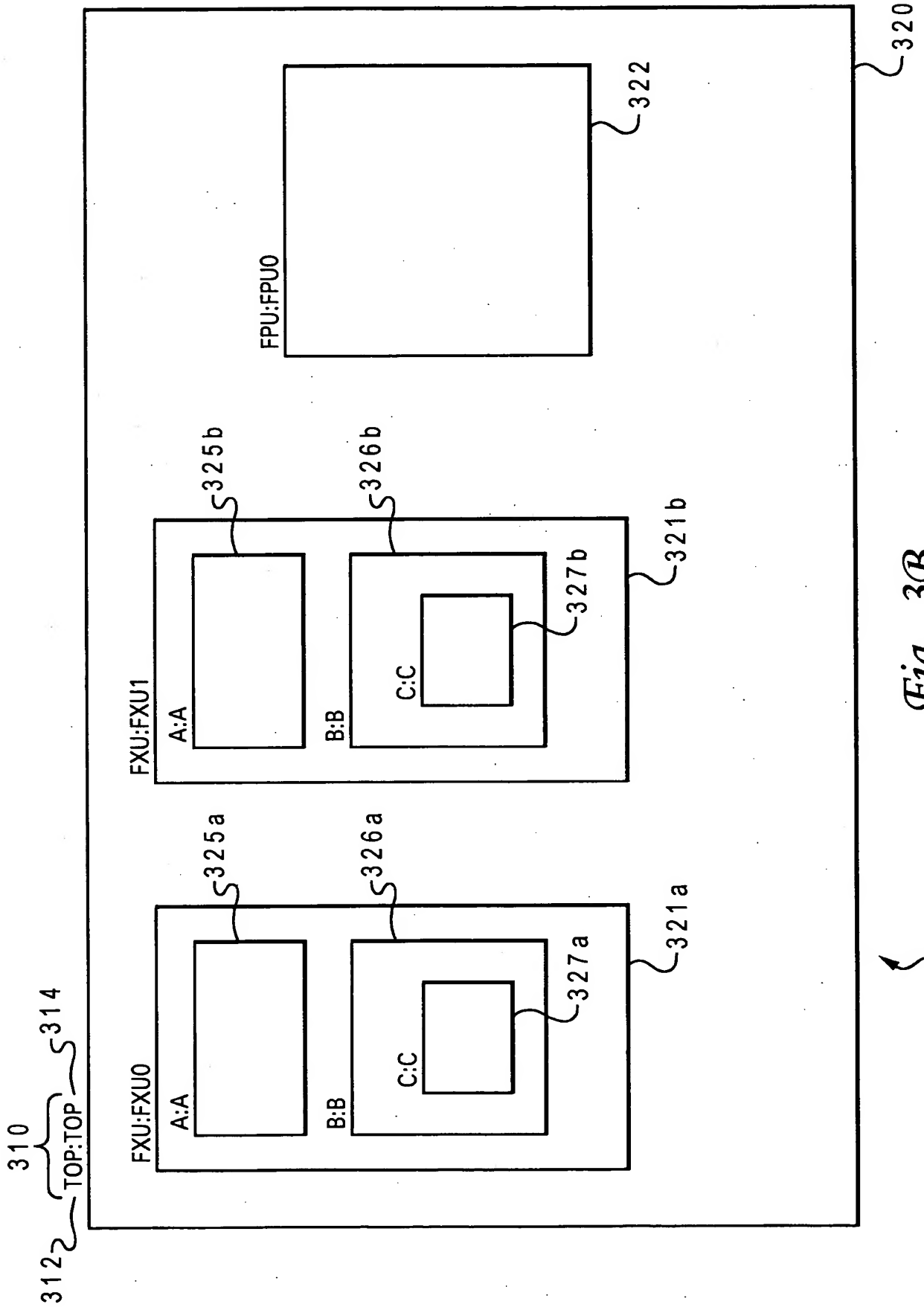
310
312
TOP:TOP
314
320
FPU:FPU0
322
FXU:FXU1
A:A
B:B
C:C
325b
326b
327b
321b
FXU:FXU0
A:A
B:B
C:C
325a
326a
327a
321a
329

Fig. 3B

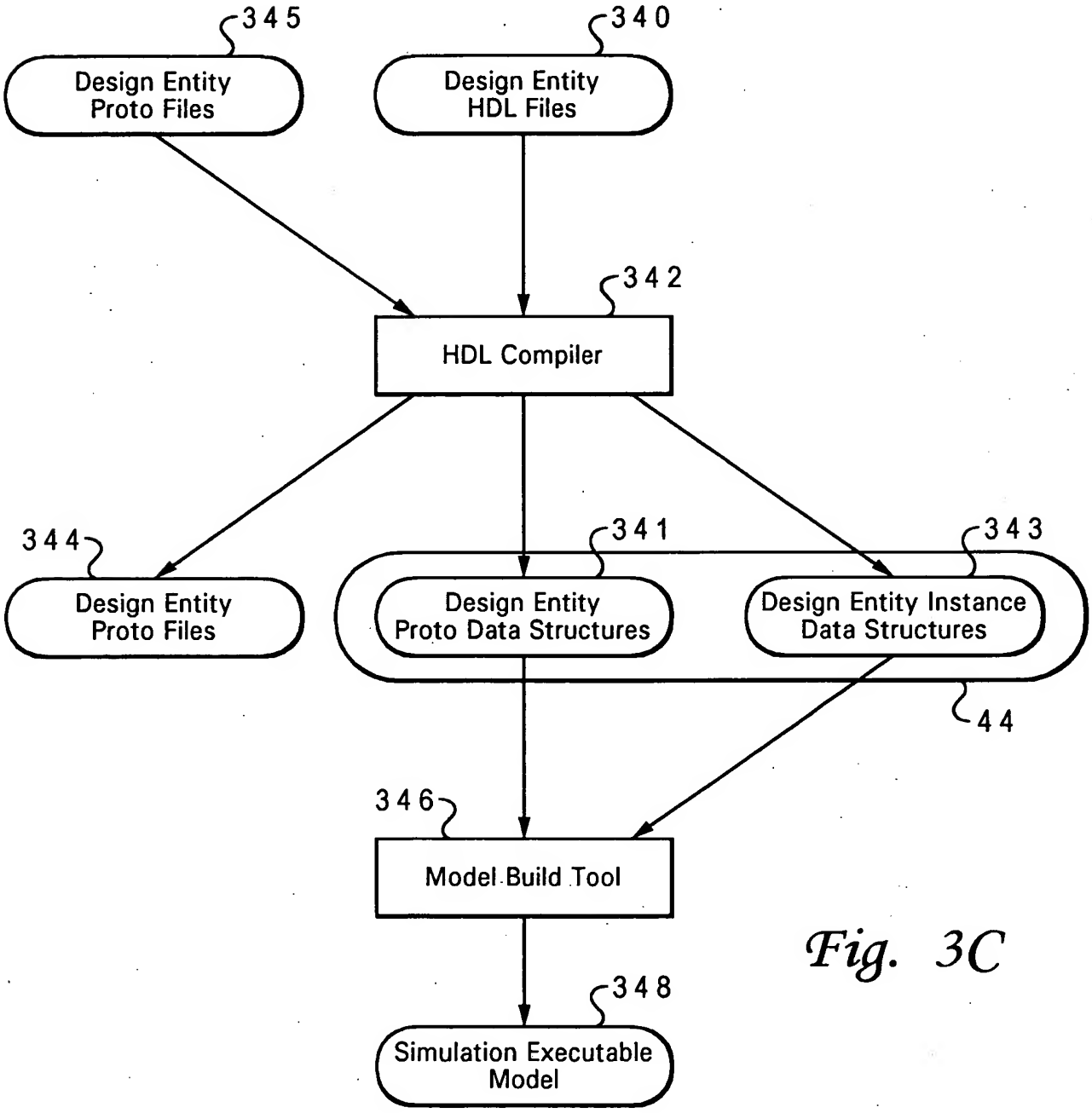
345
Design Entity Proto Files
340
Design Entity HDL Files
342
HDL Compiler
344
Design Entity Proto Files
341
Design Entity Proto Data Structures
343
Design Entity Instance Data Structures
44
346
Model Build Tool
348
Simulation Executable Model

Fig. 3C

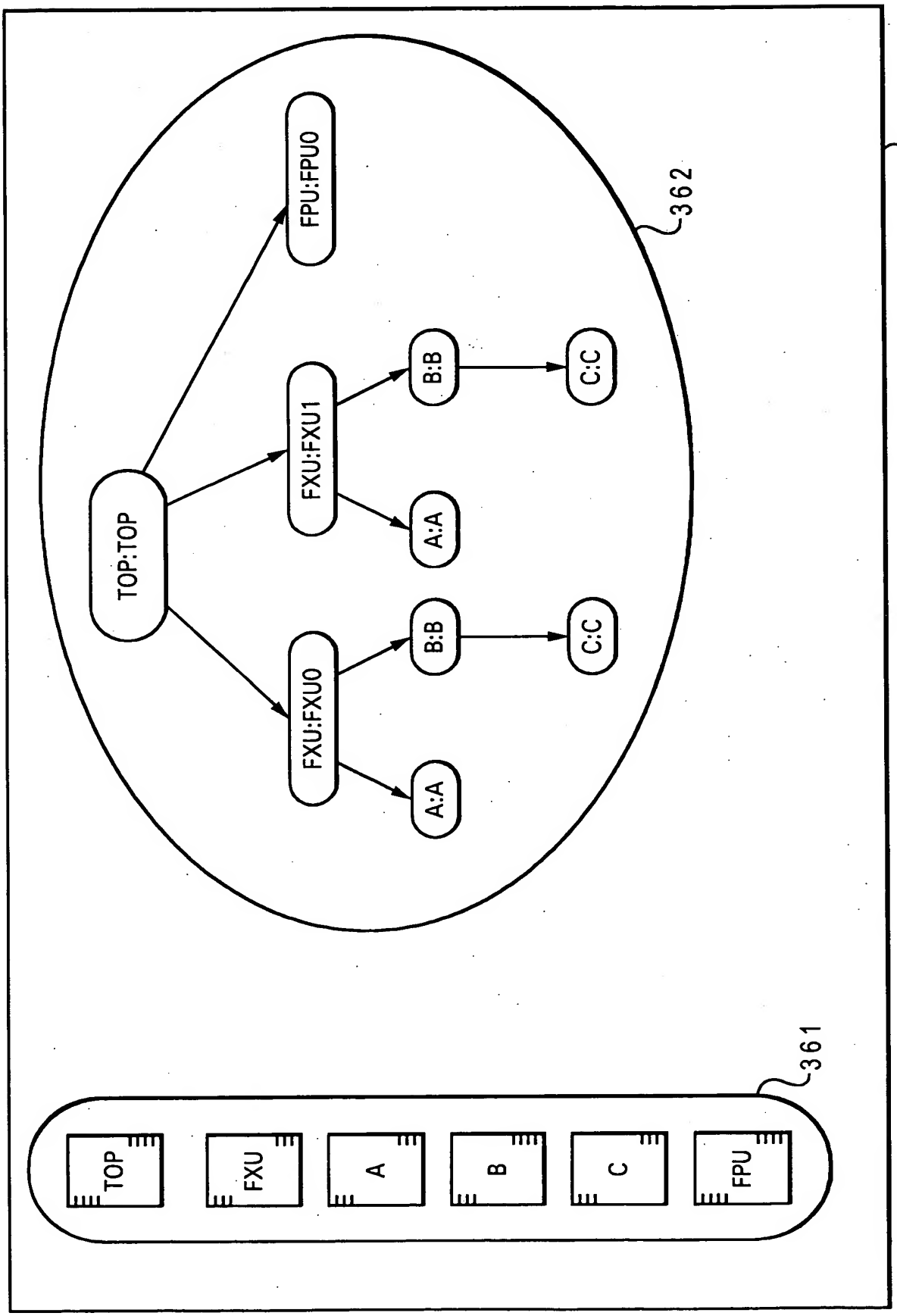
TOP
FXU
A
B
C
FPU
361
TOP:TOP
FPU:FPU0
FXU:FXU1
FXU:FXU0
A:A
B:B
C:C
A:A
B:B
C:C
362
44

Fig. 3D

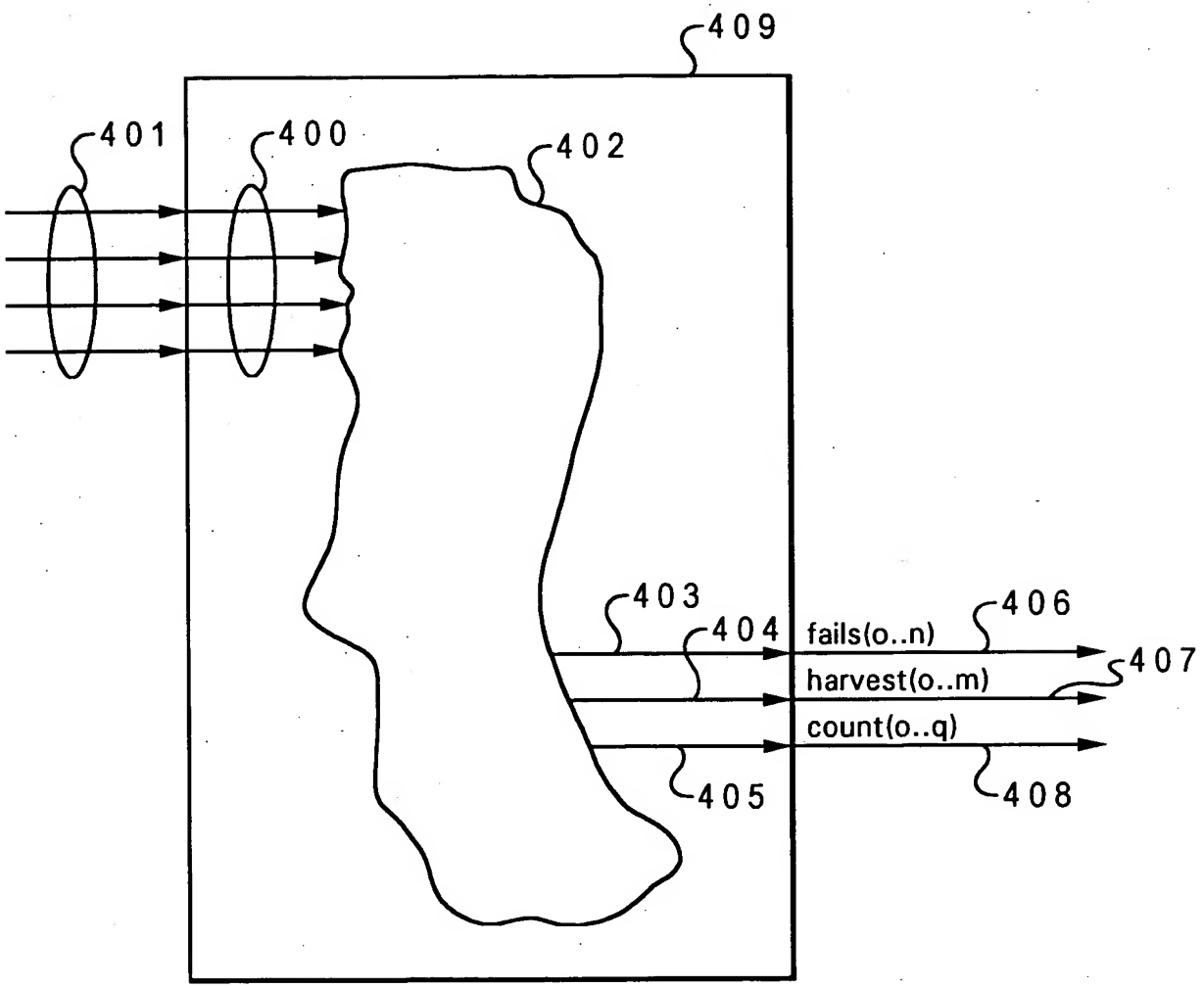
409
401
400
402
403
404
fails(o..n)
406
407
harvest(o..m)
count(o..q)
405
408

Fig. 4A

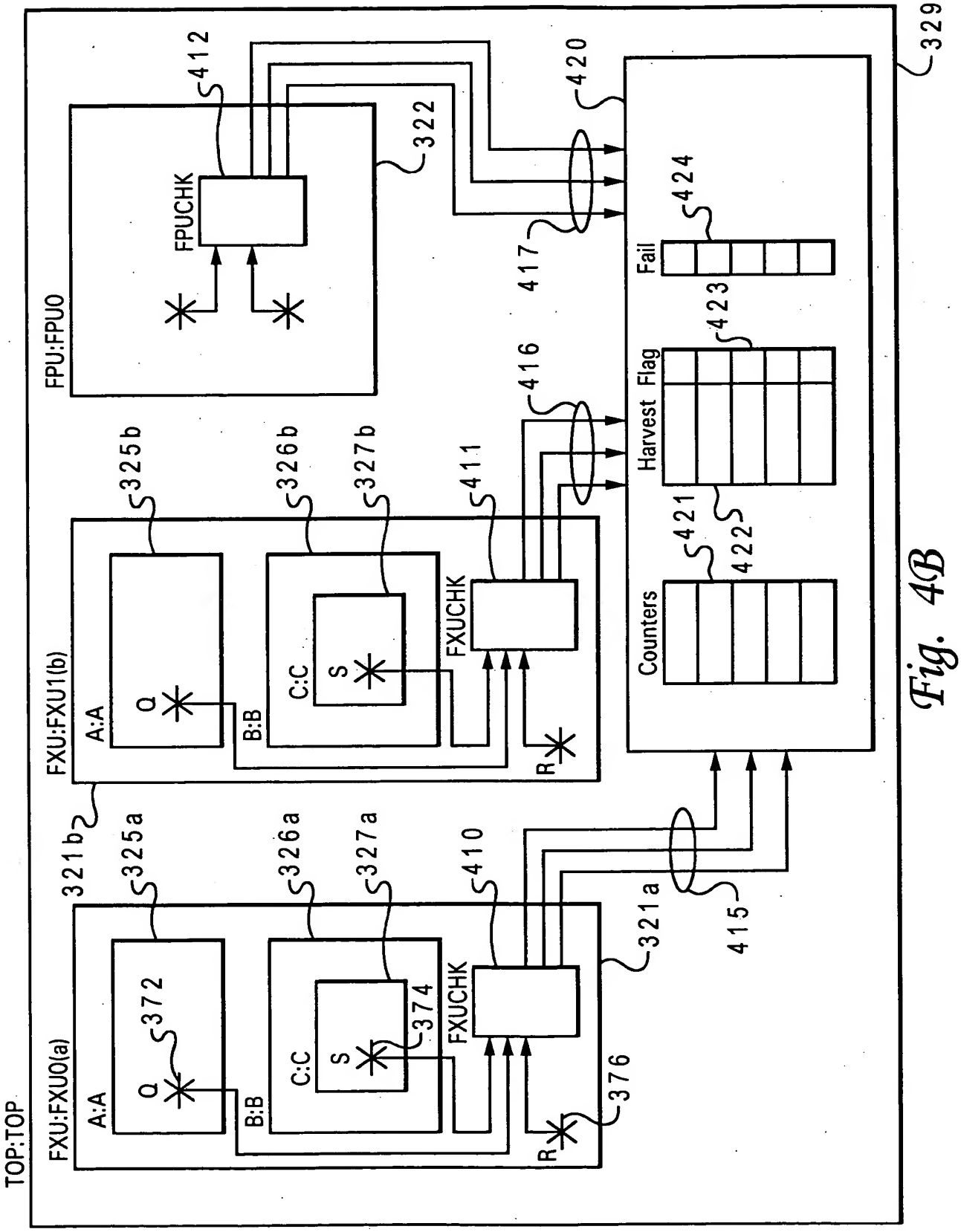
TOP:TOP
329
FXU:FXU0(a)
A:A
Q
372
B:B
C:C
S
374
FXUCHK
R
376
321a
410
326a
327a
325a
321b
FXU:FXU1(b)
411
326b
327b
325b
FPU:FPU0
FPUCHK
412
322
415
417
416
420
Counters
422
421
Harvest Flag
423
Fail
424

Fig. 4B

```
ENTITY FXUCHK IS                                                    } 450

    PORT(   S_IN        :   IN std_ulogic;                          }
            Q_IN        :   IN std_ulogic;                          }
            R_IN        :   IN std_ulogic;                          }
            clock       :   IN std_ulogic;                          }
            fails       :   OUT std_ulogic_vector(0 to 1);          }
            counts      :   OUT std_ulogic_vector(0 to 2);          }
            harvests    :   OUT std_ulogic_vector(0 to 1);          }
        );                                                          }

452 { --!! BEGIN                                                    }
    { --!! Design Entity: FXU;                                      }

    { --!! Inputs                                                   }
    { --!! S_IN       = >   B.C.S;                                  }
453 { --!! Q_IN       = >   A.Q;                                    }
    { --!! R_IN       = >   R;                                      }
    { --!! CLOCK      = >   clock;                                  }
    { --!! End Inputs                                               }

    { --!! Fail Outputs;                                            }
454 { --!! 0 : "Fail message for failure event 0";                  }
    { --!! 1 : "Fail message for failure event 1";                  }
    { --!! End Fail Outputs;                                        }  } 451

    { --!! Count Outputs;                                           }
    { --!! 0 : <event0> clock;                                      }
455 { --!! 1 : <event1> clock;                                      }
    { --!! 2 : <event2> clock;                                      }
    { --!! End Count Outputs;                                       }

    { --!! Harvest Outputs;                                         }
456 { --!! 0 : "Message for harvest event 0";                       }
    { --!! 1 : "Message for harvest event 1";                       }
    { --!! End Harvest Outputs;                                     }

457 { --!! End;                                                     }

ARCHITECTURE example of FXUCHK IS                                   }
                                                                    }
BEGIN                                                               }
                                                                    }
    ... HDL code for entity body section ...                        } 458
                                                                    }
END;                                                                }
```

Fig. 4C

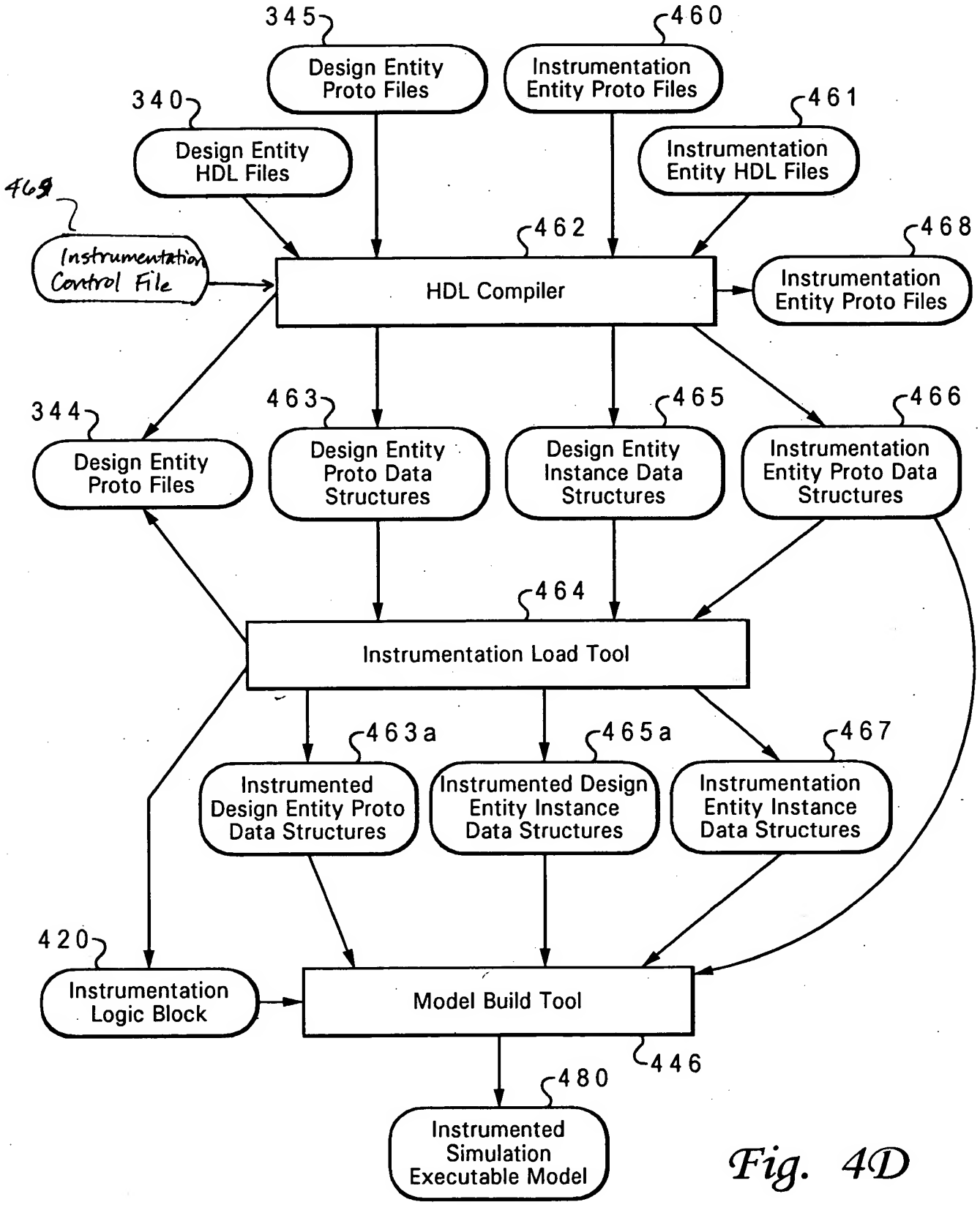
345
Design Entity Proto Files
460
Instrumentation Entity Proto Files
340
Design Entity HDL Files
461
Instrumentation Entity HDL Files
469
Instrumentation Control File
462
HDL Compiler
468
Instrumentation Entity Proto Files
344
Design Entity Proto Files
463
Design Entity Proto Data Structures
465
Design Entity Instance Data Structures
466
Instrumentation Entity Proto Data Structures
464
Instrumentation Load Tool
463a
Instrumented Design Entity Proto Data Structures
465a
Instrumented Design Entity Instance Data Structures
467
Instrumentation Entity Instance Data Structures
420
Instrumentation Logic Block
Model Build Tool
446
480
Instrumented Simulation Executable Model

Fig. 4D

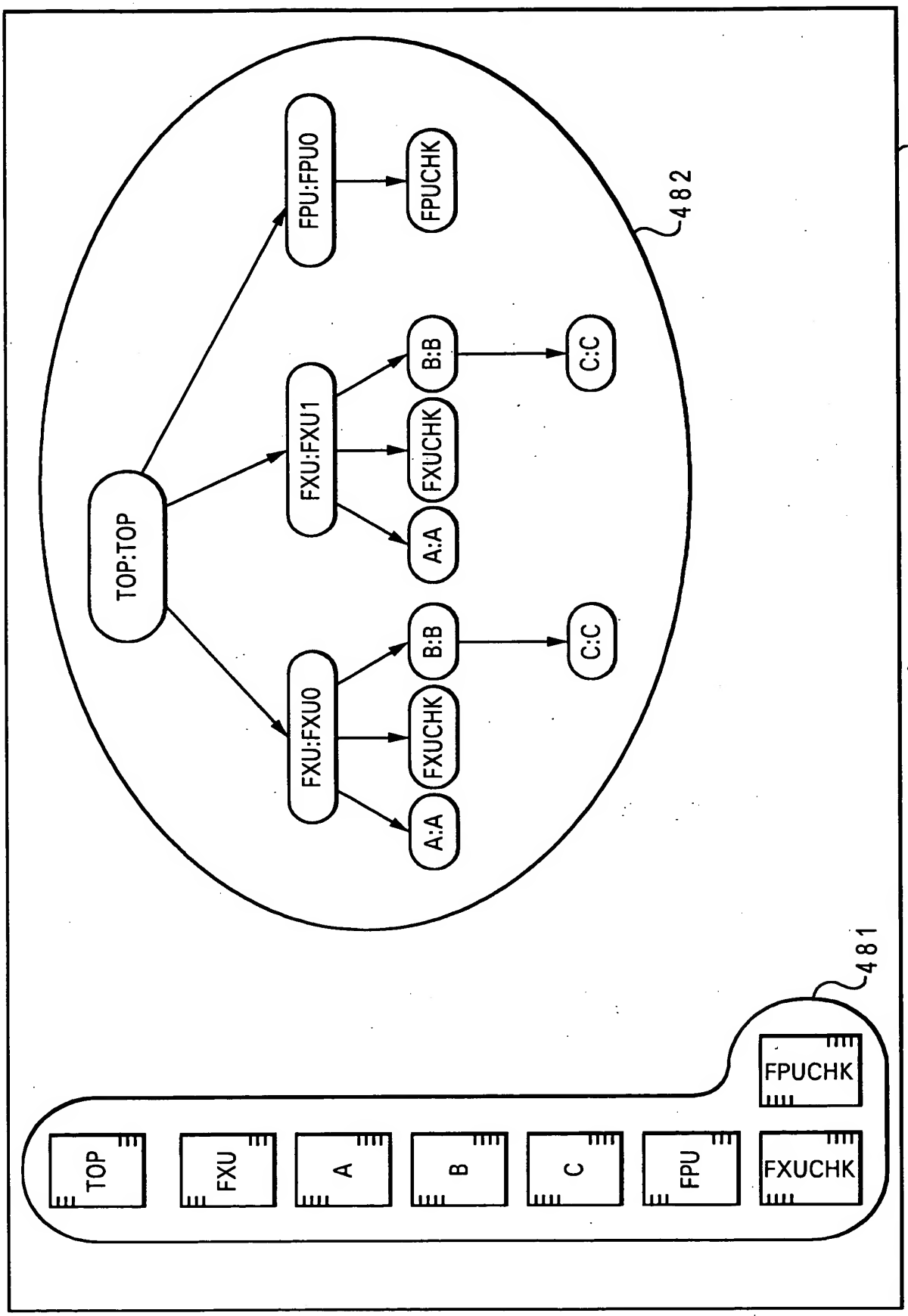
44
482
481
TOP:TOP
FPU:FPU0
FPUCHK
FXU:FXU1
B:B
C:C
FXUCHK
A:A
FXU:FXU0
B:B
C:C
FXUCHK
A:A
TOP
FXU
A
B
C
FPU
FXUCHK
FPUCHK

Fig. 4E

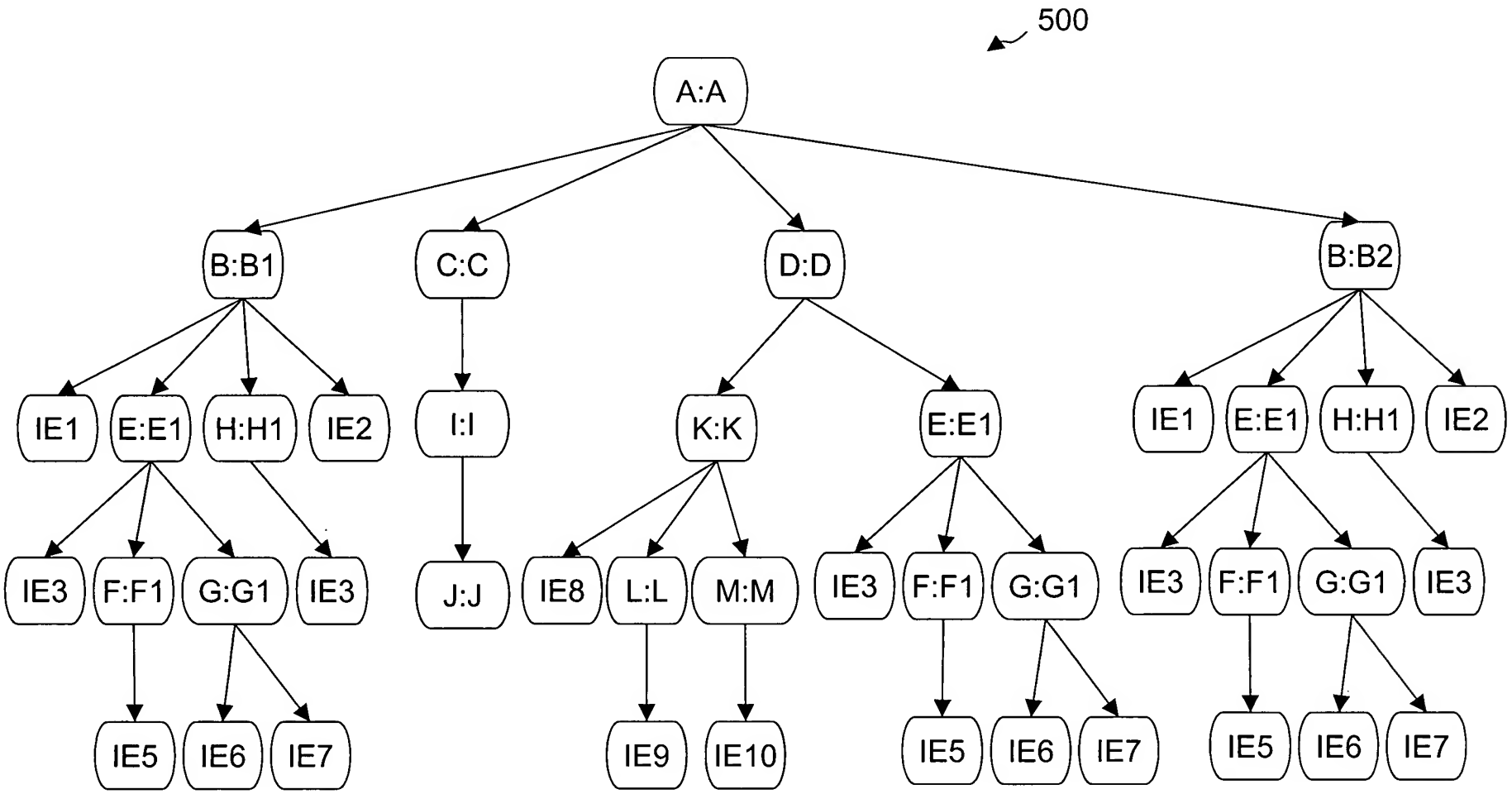
500
A:A
B:B1
C:C
D:D
B:B2
IE1
E:E1
H:H1
IE2
I:I
K:K
E:E1
IE1
E:E1
H:H1
IE2
IE3
F:F1
G:G1
IE3
J:J
IE8
L:L
M:M
IE3
F:F1
G:G1
IE3
F:F1
G:G1
IE3
IE5
IE6
IE7
IE9
IE10
IE5
IE6
IE7
IE5
IE6
IE7

FIG. 5

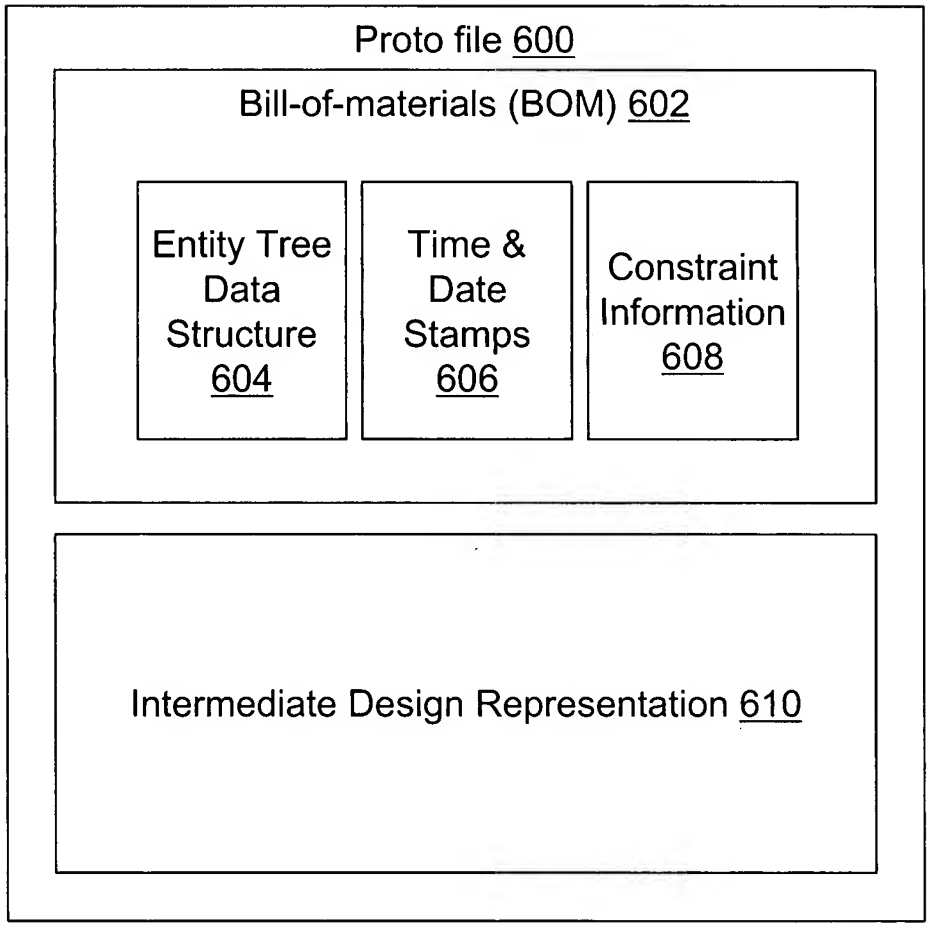
Proto file 600
Bill-of-materials (BOM) 602
Entity Tree Data Structure 604
Time & Date Stamps 606
Constraint Information 608
Intermediate Design Representation 610

FIG. 6A

604

ENTITY	DESCENDANTS
A	B, C, D
B	E, H, {IE1}, {IE2}
C	I
D	K, E
E	F, G, {IE3}
F	{IE5}
G	{IE6}, {IE7}
H	{IE4}
I	J
J	
K	L, M, {IE8}
L	{IE9}
M	{IE10}

FIG. 6B

608

ENTITY	SELECTED IEs
A	
B	
C	
D	
E	{IE3}
F	{IE5}
G	{IE6}, {IE7}
H	
I	
J	
K	
L	
M	

FIG. 6D

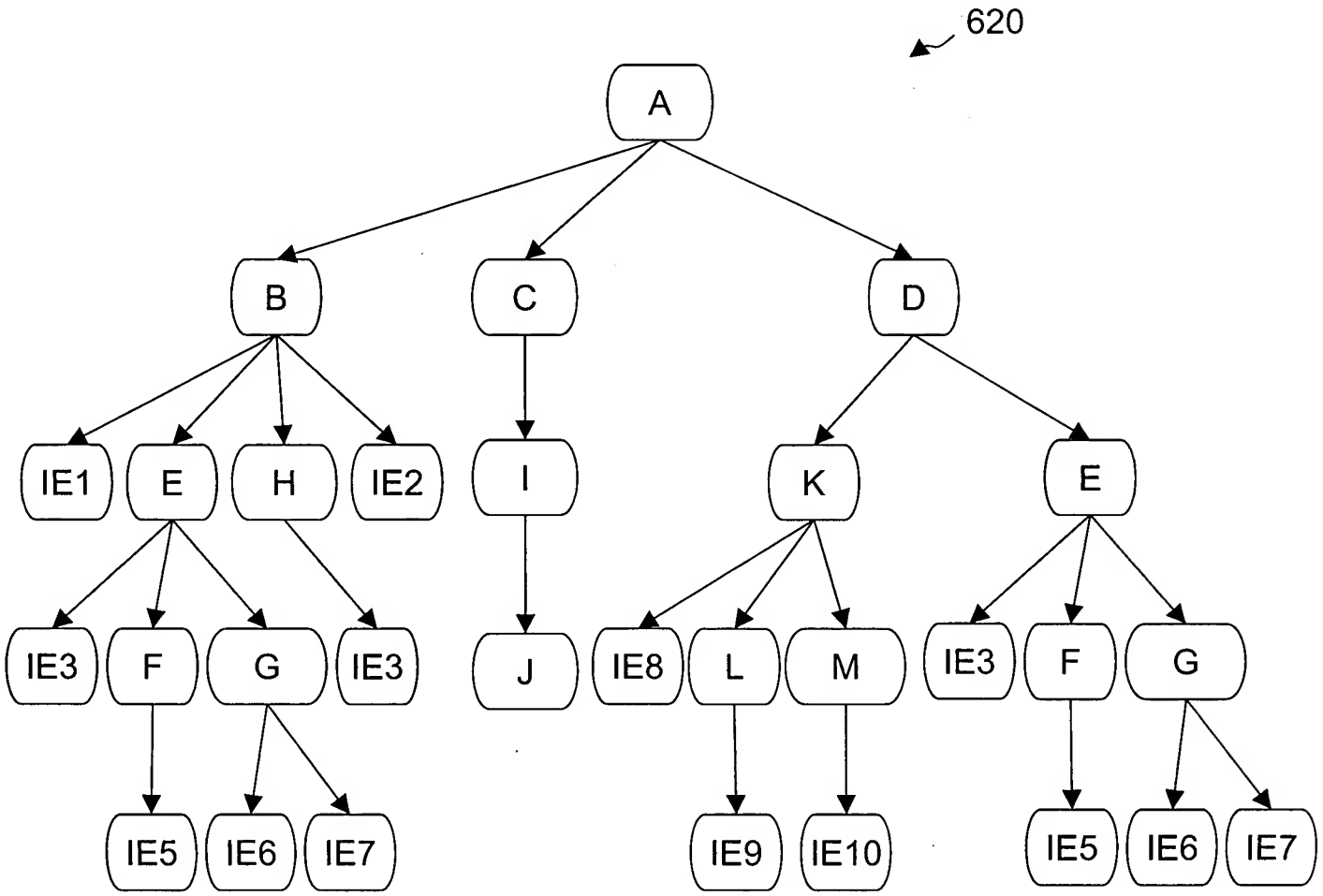
620
A
B
C
D
IE1
E
H
IE2
I
K
E
IE3
F
G
IE3
J
IE8
L
M
IE3
F
G
IE5
IE6
IE7
IE9
IE10
IE5
IE6
IE7

FIG. 6C

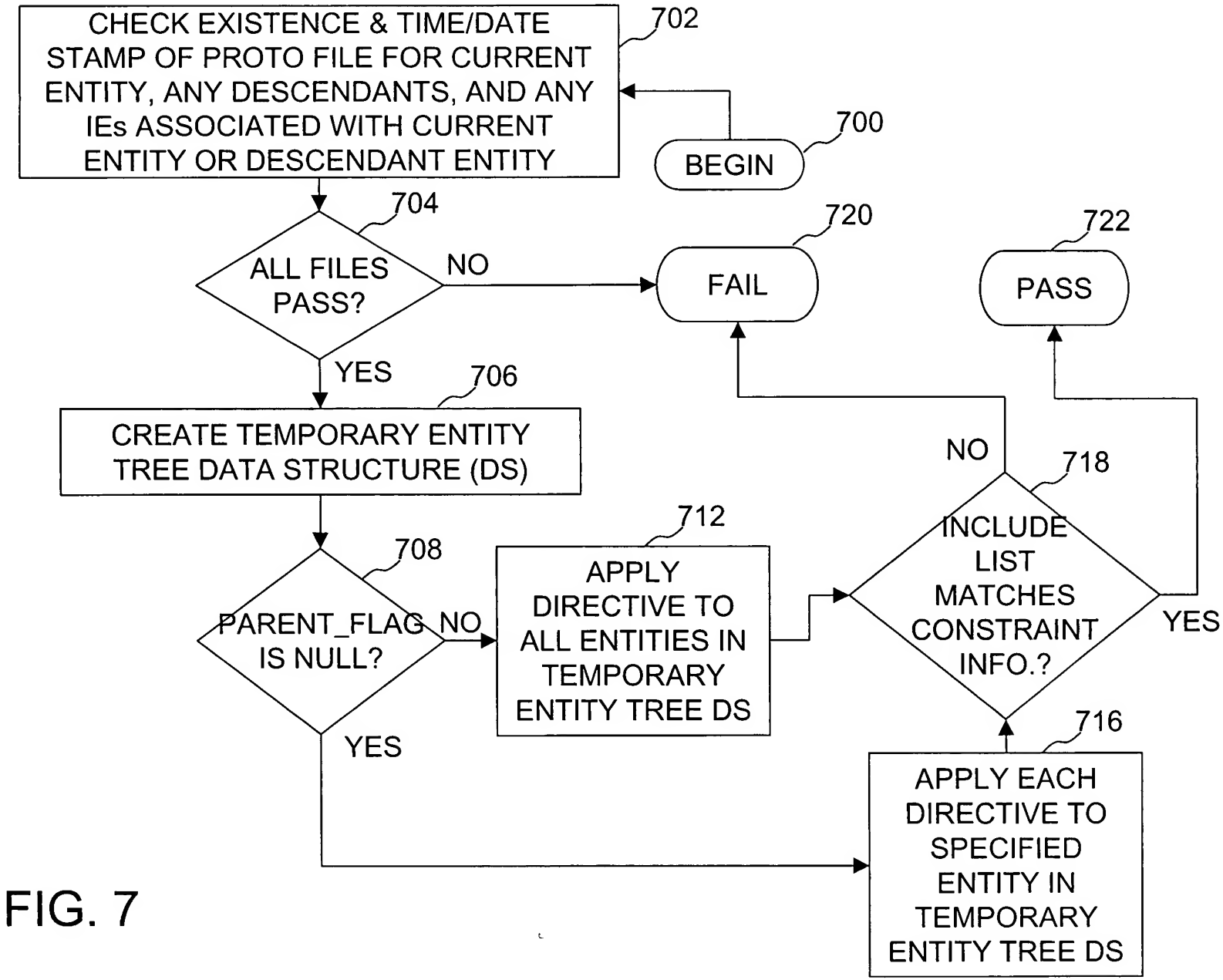
CHECK EXISTENCE & TIME/DATE STAMP OF PROTO FILE FOR CURRENT ENTITY, ANY DESCENDANTS, AND ANY IEs ASSOCIATED WITH CURRENT ENTITY OR DESCENDANT ENTITY
702
BEGIN
700
ALL FILES PASS?
704
NO
FAIL
720
PASS
722
YES
CREATE TEMPORARY ENTITY TREE DATA STRUCTURE (DS)
706
PARENT_FLAG IS NULL?
708
NO
APPLY DIRECTIVE TO ALL ENTITIES IN TEMPORARY ENTITY TREE DS
712
INCLUDE LIST MATCHES CONSTRAINT INFO.?
718
NO
YES
YES
APPLY EACH DIRECTIVE TO SPECIFIED ENTITY IN TEMPORARY ENTITY TREE DS
716

FIG. 7

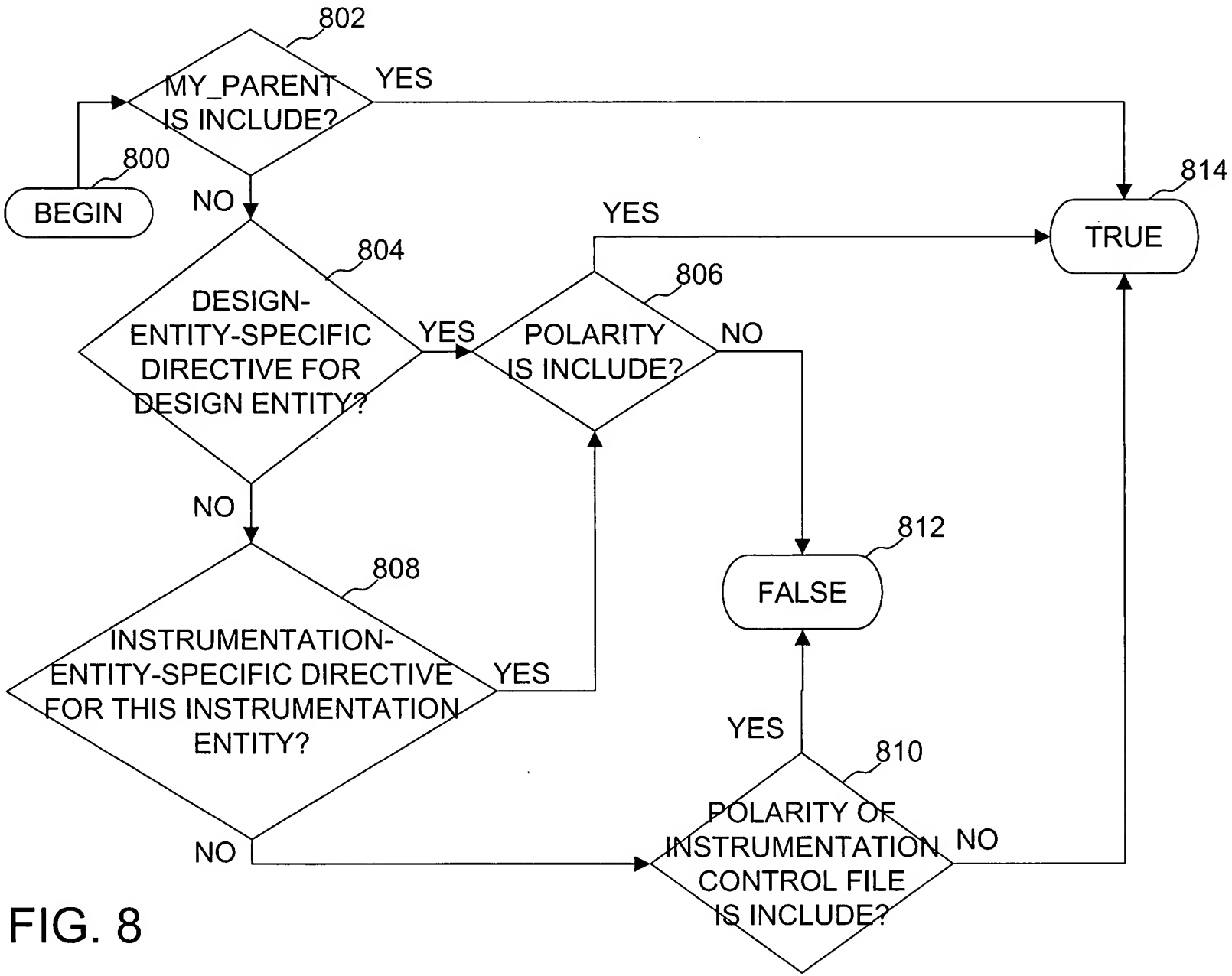
802
MY_PARENT IS INCLUDE?
YES
800
BEGIN
NO
814
TRUE
YES
804
DESIGN-ENTITY-SPECIFIC DIRECTIVE FOR DESIGN ENTITY?
YES
806
POLARITY IS INCLUDE?
NO
NO
812
FALSE
808
INSTRUMENTATION-ENTITY-SPECIFIC DIRECTIVE FOR THIS INSTRUMENTATION ENTITY?
YES
YES
810
POLARITY OF INSTRUMENTATION CONTROL FILE IS INCLUDE?
NO
NO

FIG. 8